

# **EUROPEAN PROCESSOR INITIATIVE: Europe's Industrial HPC Processor Technology for the Exascale Era**

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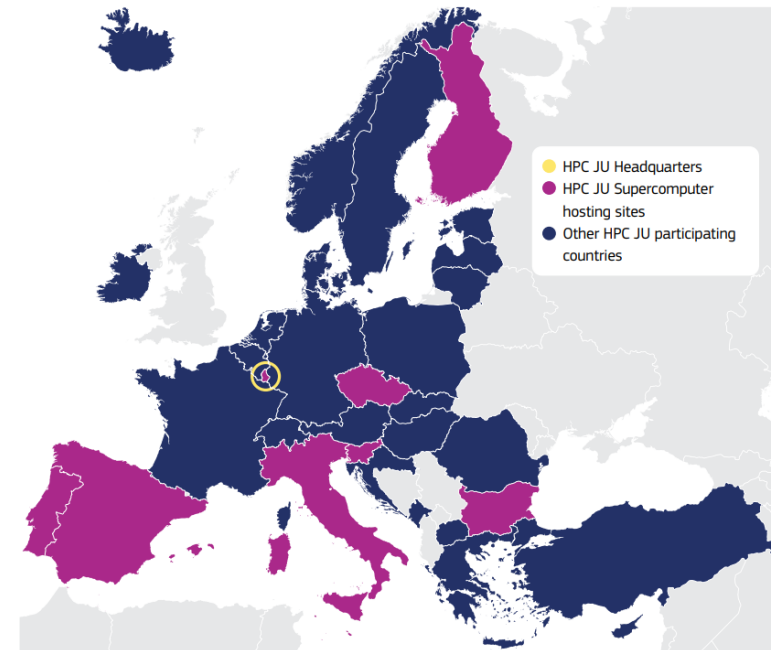


The background is a dark, textured surface covered in a dense pattern of binary code (0s and 1s). Overlaid on this are several glowing blue lines that form a complex, wavy, and interconnected pattern, resembling a stylized flower or a network of data paths. These lines have small, bright yellow-orange dots at various points, giving them a pulsating or active appearance. The overall effect is a high-tech, digital aesthetic.

# ***THE STRATEGIC INTERPLAY***

# EU EXASCALE HPC STRATEGY

- March 2017, Rome: EC launched the *EuroHPC declaration*
- November 2018, EuroHPC Joint Undertaking, a 1 billion Euro joint initiative between the EU and European countries to develop a World Class Supercomputing Ecosystem in Europe
- Oct 2020: 32 participating countries



# THE PRESIDENT OF THE EUROPEAN UNION HAS SET NEW AMBITIONS

SEPTEMBER, 16TH, 2020



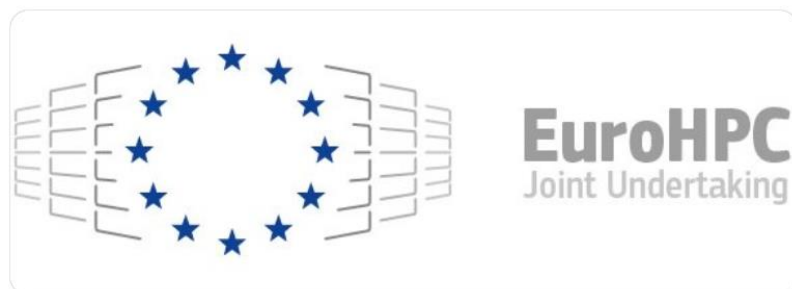
## Ursula Von Der Leyen State of the Union *Brussels – September, 16<sup>th</sup>, 2020*

- NextGenerationEU is also a unique opportunity to develop a more coherent European approach to connectivity and digital infrastructure deployment.
- None of this is an end in itself - it is about Europe's digital sovereignty, on a small and large scale.
- In this spirit, I am pleased to announce an **investment of 8 billion euros in the next generation of supercomputers** - cutting-edge technology made in Europe.
- And **we want the European industry to develop our own next-generation microprocessor** that will allow us to use the increasing data volumes energy-efficient and securely.
- This is what **Europe's Digital Decade** is all about!

[https://ec.europa.eu/commission/presscorner/detail/en/SPEECH\\_20\\_1655](https://ec.europa.eu/commission/presscorner/detail/en/SPEECH_20_1655)

# EUROHPC JU AMBITIOUS MISSION

- expand and deploy in the EU a world-class supercomputing and data infrastructure, also in view of having 3 supercomputers in the world's top 5
- make the supercomputing and quantum computing resources accessible to all users across Europe, including SMEs, and provide them with training on necessary skills
- scale up supercomputing technology to irrigate the entire digital strategy, from big data analytics and artificial intelligence, to cloud technologies and cybersecurity









# DRIVERS OF THE EPI PROPOSAL

## Societal challenges

- Climate change
- Cybersecurity
- Increasing energy needs
- Intensifying global competition
- Aging population
- Sovereignty (data, economical, embargo)

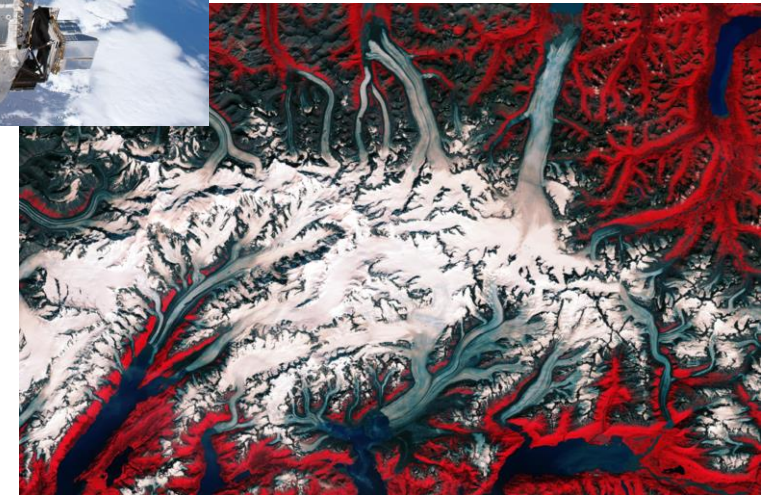


Image: <https://www.combiomed.eu/services/software-hub/>



# DRIVERS OF THE EPI PROPOSAL

- Connected mobility & *Autonomous Driving computing needs beyond 2023*
- Develop customized processors able to meet the performance needed for autonomous vehicles that would offer:
  - implementation of vehicle perception tasks in real-time in a fail-operational manner
  - increased computing performance, fail-operational, functional safety, cyber-security and real-time behaviour (RT)
  - compute resources with the same characteristics as their “big brothers” in exascale class supercomputers
- Sovereignty (data, economical, embargo)
- EU car manufacturing supremacy





# European Processor Initiative



# 28 PARTNERS FROM 10 EU COUNTRIES



# EPI OBJECTIVES

- **Overall: Develop a complete EU designed high-end microprocessor, addressing Supercomputing and edge-HPC segments**
  - Short-term objective
    - supply the EU-designed microprocessor to empower the EU Exascale machines
  - Long-term objective
    - Europe needs a sovereign (=not at risk of limitation or embargo by non-EU countries) access to high-performance, low-power microprocessors, from IP to products
  - EPI has been set to fulfil this objective
  - EPI has to cover all Technical Readiness levels (TRL)
    - TRL 1-3 are for long-term objectives (EU IP)
- \*and\***
- TRL 4-9 are for short to mid-term objectives (decade) with products designed in EU







# MERGE OF HPC AND AI

# HPC BEFORE ARTIFICIAL INTELLIGENCE

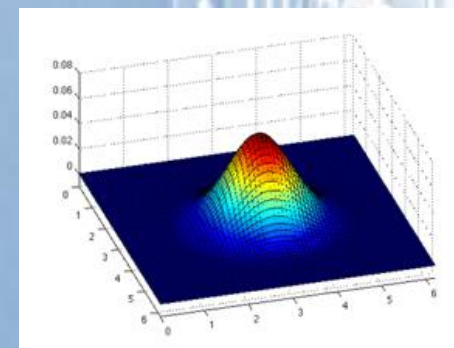
Theoretical model → HPC Application → Results

$$\frac{\partial u}{\partial t} = k \frac{\partial^2 u}{\partial x^2}$$

```

190 C      PIN=0.02
191 IF(DOT.NE.0.0) THEN
192   DT=DOT
193 ELSE
194   DT=PIN
195 ENDIF
196 WRITE(*, '(A)') ' PLEASE ENTER NAME OF OUTPUT FILE (FOR EXAMPLE
197 * B123.DAT)'
198 READ(*, '(A)') FNAMEO
199 OPEN(6, FILE=FNAMEO, STATUS='UNKNOWN')
200 F0=WFIX/TH
201 F0=REQ*F0/TH
202 C0=CS
203 C
204 C      TIME=0.000
205 EF=0.500
206 5 CONTINUE
207 GAMMA=DT/(2.00*DX*DX)
208 BETA=DT/DX
209 IF((BETA*FV).GT.0.5000) GO TO 7
210 IF((GAMMA*F0)/(BETA*FV)).LT.0.500) GO TO 6
211 GO TO 8
212 6 DX=DX/2
213 GO TO 5
214 7 DT=DT/2
215 GO TO 5
216 8 CONTINUE
217 N=COL/DX
218 NH1=N-1
219 NH2=N-2
220 NH1=N+1
221 GAMMA=DT/(2*DX*DX)
222

```





# HPC WITH ARTIFICIAL INTELLIGENCE

Theoretical model → HPC Application

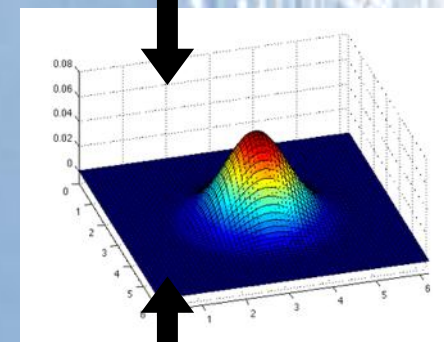
$$\frac{\partial u}{\partial t} = k \frac{\partial^2 u}{\partial x^2}$$

```

190 C      FIM=0.02
191 IF (DOT.NE.0.0) THEN
192   DT=DOT
193 ELSE
194   DT=1M
195 ENDIF
196 WRITE(*, '(A)') ' PLEASE ENTER NAME OF OUTPUT FILE (FOR EXAMPLE
197 *  A121.DAT)'
198 READ(*, '(A)') FRAMED
199 OPEN(4, FILE=FRAMED, STATUS='UNKNOWN')
200 P=HRESL/TH
201 RS=REQ*ROU*RO/TH
202 CPCS
203 C
204 TIME=0.000
205 EF=0.000
206 CONTINUE
207 GAMMA=DT/(2.00*DX*DX)
208 BETA=DT/DS
209 IF (BETA*PV).GT.0.5000) GO TO 1
210 IF (GAMMA*D/(BETA*PV)).LT.0.500) GO TO 6
211 GO TO 8
212 6 DX=DX/2
213 GO TO 5
214 7 DT=DT/2
215 GO TO 5
216 8 CONTINUE
217 M=COL/DX
218 NN1=M-1
219 NN2=M-2
220 NP1=M-1
221 GAMMA=DT/(2*DX*DX)
222

```

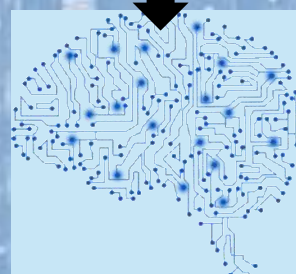
Results



Results




Big Data



AI





# Cambrian explosion

## Achieving performance through specialization

Courtesy Steve Scott  
Cray CTO

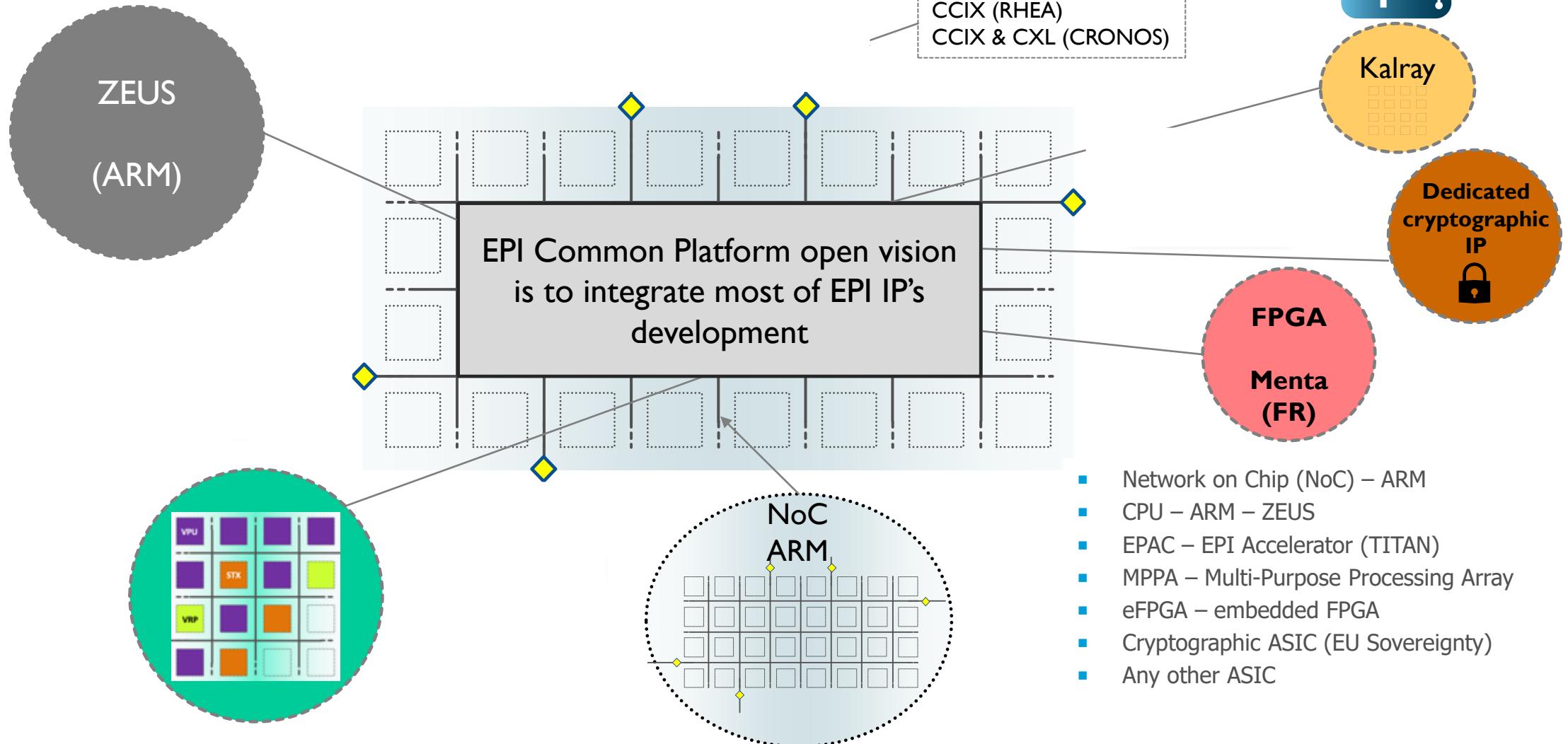


## TOP10 (GREEN) OVER THE LAST 10 YEARS

	2009 – Nov.	2014 – Nov.	2020 – Nov.	(Post) Exascale
CPU <u>only</u>	9	5	2	0
CPU + ACC.	1	5	8	10

# ***THE EPI TECHNOLOGY: COMMON PLATFORM***

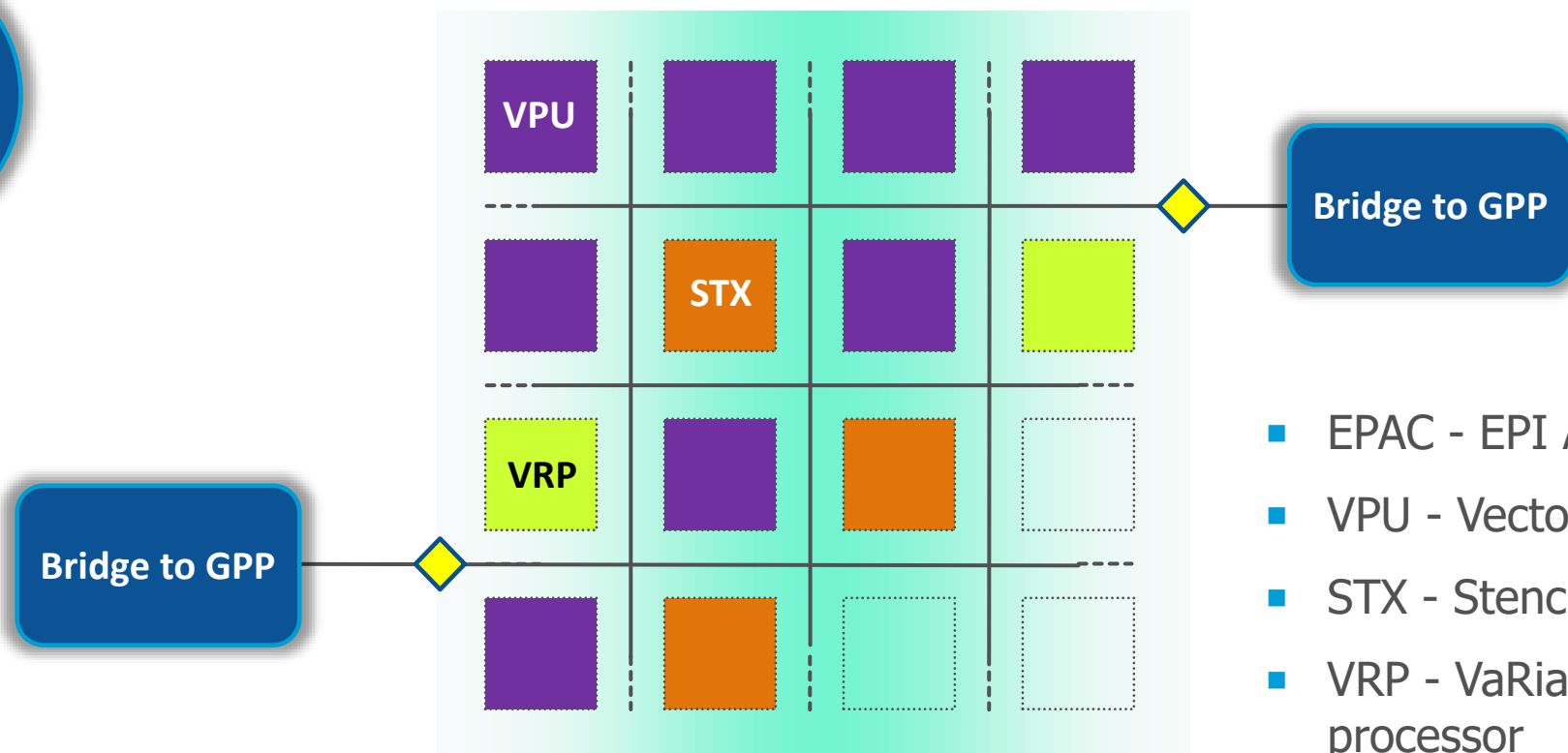
# GPP AND COMMON ARCHITECTURE





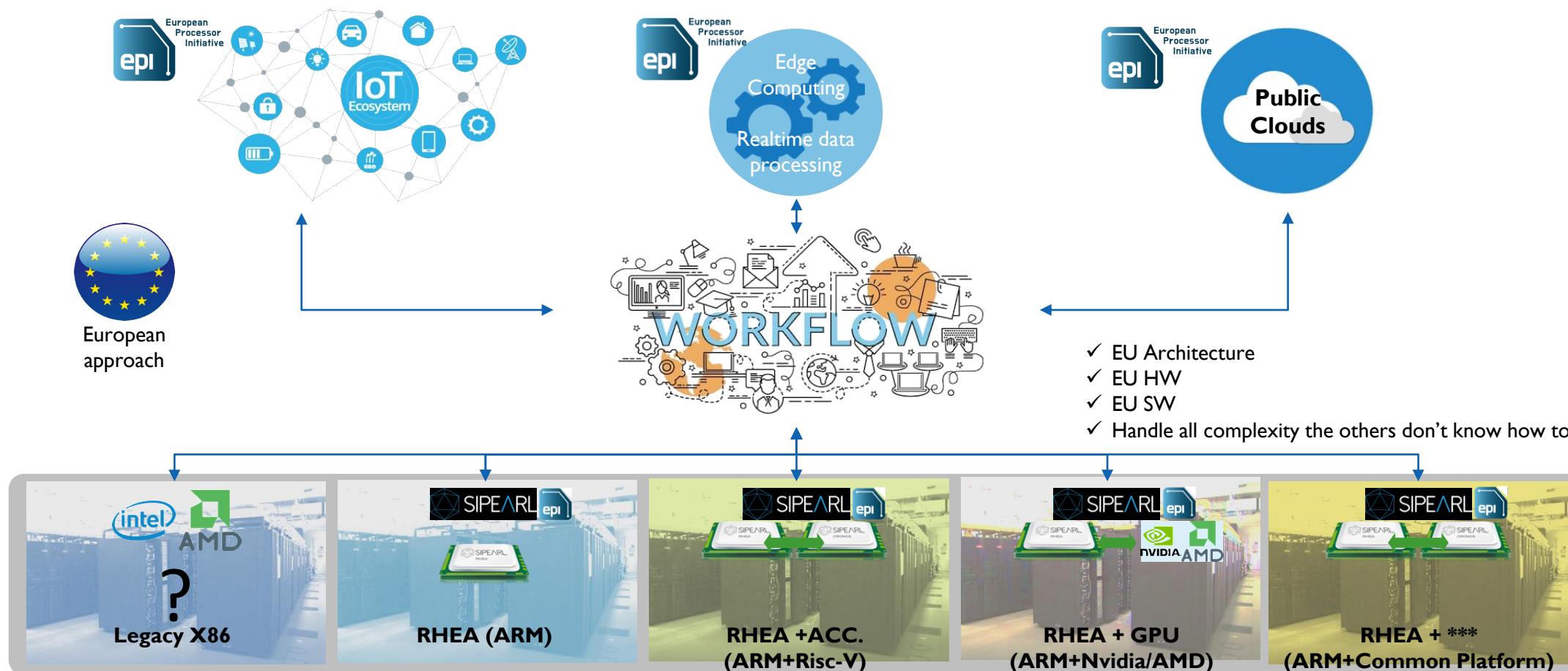
# ***THE EPI TECHNOLOGY: ACCELERATORS***

# EPAC – RISC-V ACCELERATOR FOUNDATIONS

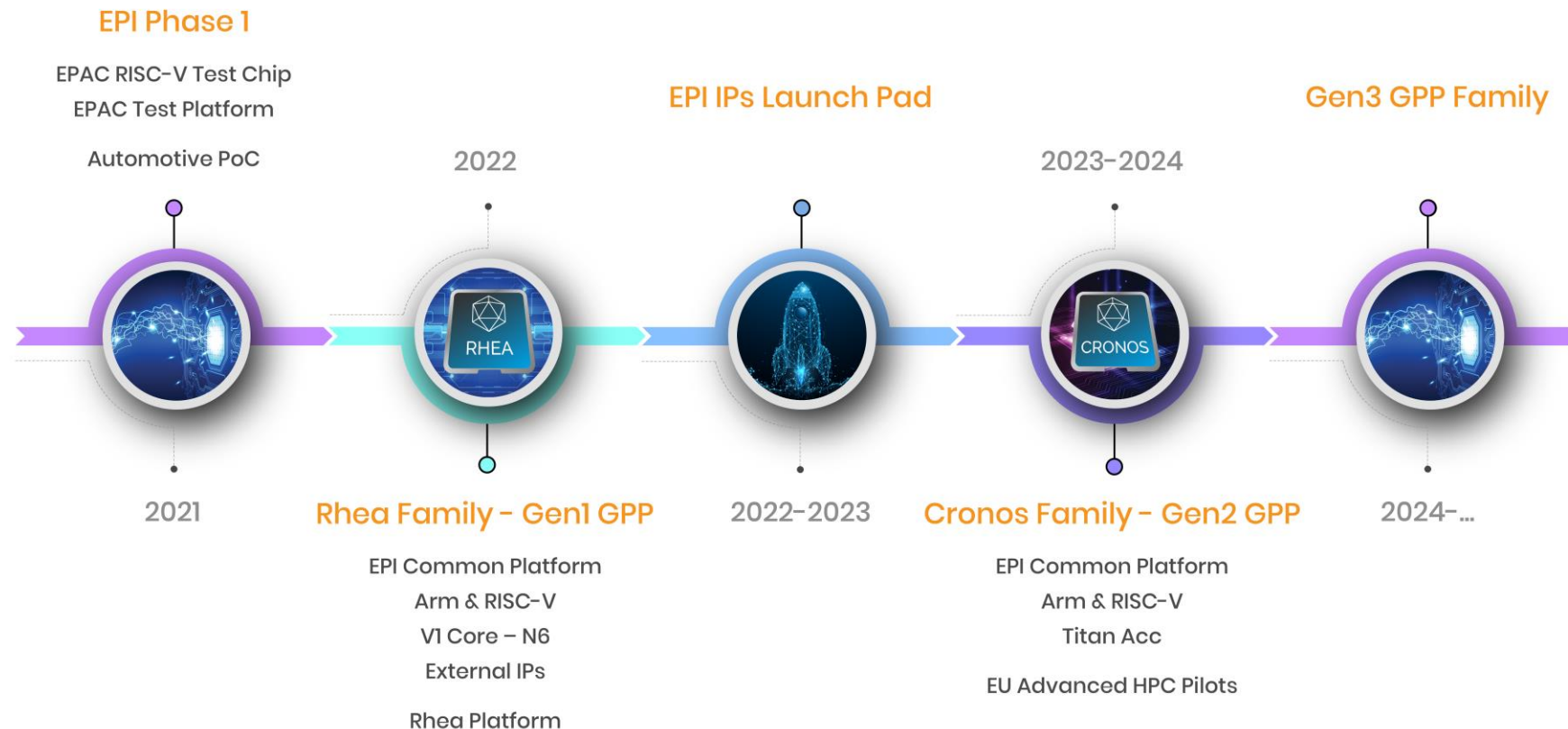


- EPAC - EPI Accelerator
- VPU - Vector Processing Unit
- STX - Stencil/Tensor accelerator
- VRP - VaRIable Precision co-processor

# THE EPI EU APPROACH







# EPI ROADMAP

## TO CONCLUDE

- Use of HPC and AI is cornerstone of successful address of societal and global challenges
- Future science, technologies and applications require processing of vast amount of data and there is a large need for efficient HPC
- HPC provides needed competitiveness for industry and society
- The expertise for developing high-end and complex processing units in Europe, after decades of dis-investment
- The European Processor Initiative aims to provide an EU HPC processor, accelerators and system/application design for exascale HPC systems in Europe and around the globe



# THANK YOU FOR YOUR ATTENTION



# European Processor Initiative



[www.european-processor-initiative.eu](http://www.european-processor-initiative.eu)



@EuProcessor



## European Processor Initiative



## European Processor Initiative