EPI EPAC1.0 RISC-V core boots Linux on FPGA

The European Processor Initiative (EPI) https://www.european-processor-initiative.eu/, a project with 28 partners from 10 European countries, with the goal of helping the EU achieve independence in HPC technologies is proud to announce that we have successfully booted Linux on our EPAC 1.0 core subset implemented on FPGA.

One key segment of EPI activities is to develop and demonstrate fully European processor IPs based on the RISC-V Instruction Set Architecture, providing power efficient and high throughput accelerator core named EPAC (European Processor Accelerator). Using RISC-V will allow leveraging open-source resources at hardware architecture level and software level, as well as ensuring independence from non-European patented computing technologies.

First silicon implementation of EPAC 1.0 test chip is expected in the second half of 2021 and as an important technical milestone towards that goal, we have successfully booted Linux on a subset of EPAC 1.0 synthesized on FPGA. The FPGA design includes the Avispado RISC-V core, the Vector Processing Unit (VPU), the Network on Chip (NoC), the Shared L2 Cache with Coherence Home Node (L2HN), interrupt controllers, IO peripherals and several other components. This implementation will enormously speed-up software development on the EPI HPC architecture as well as testing and improving the architecture for next generations EPAC chips.

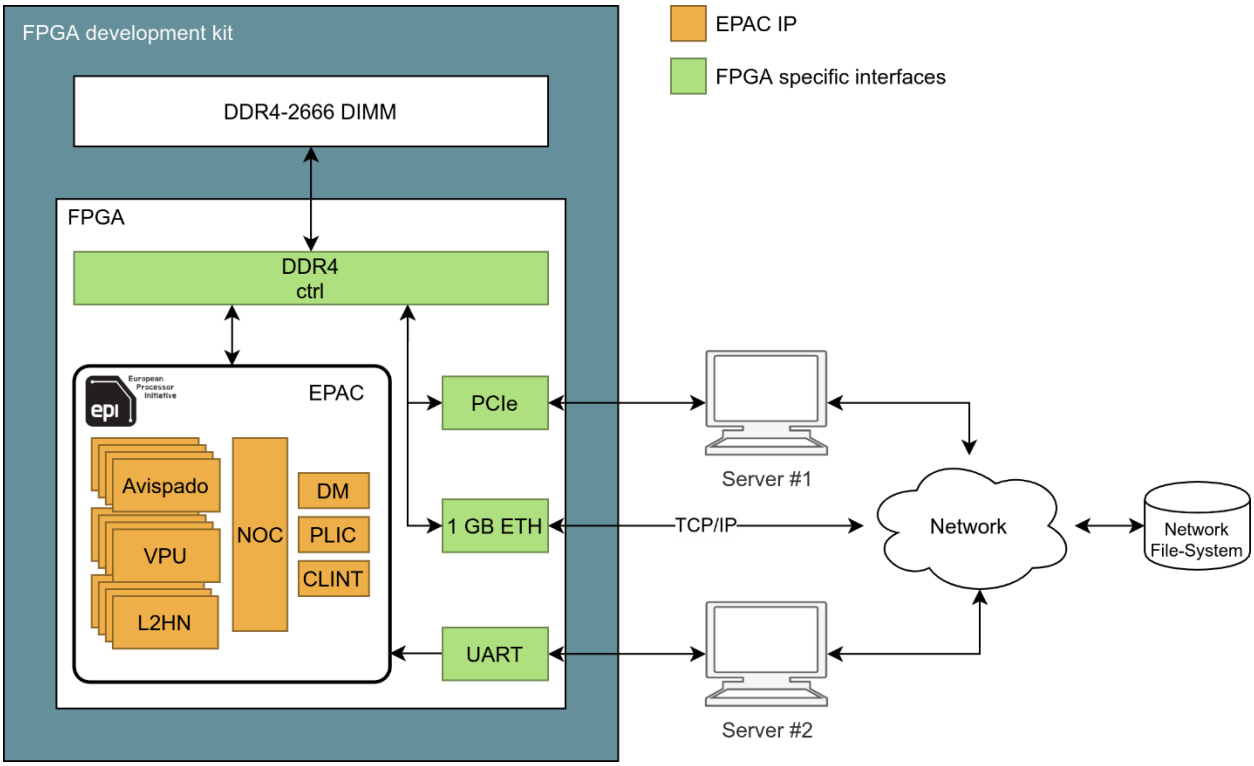

Figure 1 FPGA emulation and EPAC Software Development Vehicle block diagram

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For the development of the EPI Accelerator Test Chip, we make extensive use of FPGA technologies to verify the RTL design of the Test Chip. The subset of EPAC 1.0 emulated on FPGA we use as Software Development Vehicle (SDV) to enable early software development before the actual Test Chip silicon comes back from the foundry.

The use of FPGAs enables the testing of RTL blocks with real and very complex software in timescales that are not tractable using pure RTL simulation. Also, it allowed us to stress memory coherence and several related corner cases. We have managed to boot Linux using the EPAC 1.0 system on FPGA and the system boots within a few dozens of seconds compared to weeks using pure simulation. The system is fully usable and interactive for system software and application development and it also includes Ethernet connectivity to enable running large and complex software packages, e.g., OpenMP, MPI.

This is a serious proof of concept that gives us the confidence of a functional and viable future product.

More details on the results can also be found on EPI YouTube Channel, where you can find the second episode of EPI Talks podcast, themed with booting Linux:

Channel: https://www.youtube.com/c/EuropeanProcessorInitiative/featured

Video: https://www.youtube.com/watch?v=X4klPnBjstI

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